IN THE CLAIMS

Please amend claims 1-8 as follows:

1. (Currently Amended) A processor comprising:

a register file including a plurality of registers assigned with register numbers, each of the registers storing operand data;

a plurality of operation pipes, each operation pipe for executing in parallel one kind of operation on a plurality of the operand data;

a decoder for decoding a register designating field of an instruction code, said register designating field having a register number stored therewith, said decoder further for generating signals designating register numbers based on the register number of the register designating field, said designated register numbers being consecutive with the register number of the register designating field; and

a control circuit for sending operand data stored in the registers corresponding to the designated register numbers to at least one of the operation pipes such that said at least one of the operation pipes executes in parallel the one kind of operation associated therewith on the operand data sent from the corresponding designated registers ~~including an operation instruction comprising an instruction code and at least one register designating field, wherein the at least one register designating field is capable of designating a plurality of registers having consecutive numbers~~.

2. (Currently Amended) A processor comprising:

a register file including a plurality of registers assigned with register numbers;

a plurality of operation pipes, each operation pipe for executing in parallel one kind of operation on a plurality of operand data so as to generate operation result data;

a decoder for decoding a register designating field of an instruction code, said register designating field having a register number stored therewith, said decoder further for generating signals designating register numbers based on and consecutive with the register number of the register designating field, and the registers corresponding to the designated register numbers being designated for storing the operation result data; and

a control circuit for sending the operation result data from at least one of the operation pipes to the corresponding designated registers

~~a decoder designating a plurality of read registers in one field in an arbitrary number of register designating fields; and~~

~~a register file for outputting data in a plurality of registers having consecutive numbers in accordance with an output from the decoder~~.

3. (Currently Amended) A processor comprising:

a register file including a plurality of registers assigned with register numbers, each of the registers for storing at least one of operand data and operation result data;

a plurality of operation pipes, each operation pipe for executing in parallel one kind of operation on a plurality of the operand data so as to generate the operation result data;

a first decoder for decoding a first register designating field of an instruction code, said first register designating field having a first register number stored therewith, said first decoder further for generating signals designating source register numbers based on and consecutive with the first register number;

a second decoder for decoding a second register designating field of the instruction code, said second register designating field having a second register number stored therewith, said second decoder further for generating signals designating result register numbers based on and consecutive with the second register number; and

a control circuit for sending the operand data stored in source registers corresponding to the designated source register numbers to at least one of the operation pipes such that said at least one of the operation pipes executes in parallel the one kind of operation associated therewith on the operand data and for sending the operation result data obtained from the at least one operation pipe to result registers corresponding to the designated result register numbers

~~a decoder for designating a plurality of write registers in one field in an arbitrary number of register designating fields; and~~

~~a register file capable of writing values in a plurality of registers having consecutive numbers in accordance with an output from the decoder~~.

4. (Currently Amended) The processor according to Claim [[2]] 3, wherein the plurality of registers ~~file includes~~ are divided into a plurality of banks, and by reading or writing data

from the plurality of banks, the number of ports of reading or writing the data of [[the]] respective banks is restricted to be equal to or smaller than [[the]] a number of the register designating fields[[,]] so as to ~~thereby~~ restrain an increase in a circuit scale caused by reading or writing the data by a number of times larger than the number of the register designating fields contained in the instruction code.

5. (Currently Amended) The processor according to Claim 1, wherein the number of the plurality of registers ~~having the consecutive number~~ is limited to the n-th power of 2 [[(]] where n is a natural number[[)]], ~~to thereby enable~~ so as to reduce register selecting circuits.

6. (Currently Amended) The processor according to Claim [[1]] 3, wherein a data pack operation, which ~~is capable of dealing~~ deals with a number of the data read from the [[read]] source registers larger than a number of the data written to the [[write]] result registers, ~~in order to read~~ data read from the source registers are larger in a number than [[the]] a number of the ~~read~~ register designating fields contained in the instruction code so as to eliminate~~, is realized without producing~~ invalid portions in the [[write]] result registers.

7. (Currently Amended) The processor according to Claim [[1]] 3, wherein a data unpack operation, which ~~is capable of dealing~~ deals with a number of the data written to the [[write]] result registers larger than a number of the data read from the [[read]] source registers, ~~such that the~~ a number of data ~~can be~~ written in parallel to the result registers is larger ~~in a number~~ than [[the]] a number of the ~~write~~ register designating fields contained in the instruction code so as to avoid~~, is realized in parallel without executing~~ data writing a plurality of times.

8. (Currently Amended) The processor according to Claim [[1]] 3, wherein an operation of outputting the data having a data width wider than a width of input data such that [[the]] a number of data ~~can be written to the registers~~ larger ~~in a number~~ than [[the]] a number of the write register designating fields contained in the instruction code can be written to the results registers so as to eliminate~~, is realized without producing an~~ invalid portions in the input data and ~~without~~ avoid mounting a special register having a wider data width.